9.6 An Adaptive Low-Jitter LC-Based Clock Distribution

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High-frequency and low-jitter clocks are a critical part of digital and mixed-signal systems. In addition to generating a high-fidelity clock signal from a PLL, the clock must also be distributed with little added noise either from the intrinsic thermal noise or from supply variations. Recent demonstrations of low-noise clock distribution use LC-based clock networks [1-5]. These topologies are classified either as injection-locked oscillators or as LC-resonant clock trees. This paper proposes a new clock distribution architecture that adaptively blends these two topologies to minimize jitter. Since the LC resonant frequency substantially impacts the jitter performance, the paper also describes an automated tuning technique for the LC resonant frequency that maximizes the voltage swing using a voltage-swing digitizer. Figure 9.6.1 shows a system diagram of the proposed clock distribution.

The topology of the global clock driver is shown in Fig. 9.6.2. The current ratio between the input and the positive-feedback stage is adjustable through digital control. This current adjustment enables us to (a) evaluate and compare the two topologies, and (b) optimize the current setting for minimum jitter for a given power dissipation.

Intuitively, when the current ratio favors the positive feedback, the circuit approaches an injection-locked oscillator and more noise inherent to the global clock buffer appears at the output due to larger equivalent parallel resistance while the output signal power stays constant. Similarly, with the input frequency close to the LC-resonant frequency, when the current ratio favors the input transconductance, more input noise appears at the output due to the increased noise bandwidth.

Four possible noise conditions are shown in Fig. 9.6.3. In each case, the input to the global clock buffer is assumed to have a phase noise with 20dB/dec roll-off such as one from an oscillator or PLL. The two noise sources from the positive feedback and the input are separately shown. The multiple lines represent increasing the current in favor of the positive feedback. In case I, the input noise contribution is higher than the inherent noise of the clock buffer regardless of the digital current setting. So, the clock buffer is configured as an injection-locked oscillator. Case II describes the opposite scenario where the circuit is configured optimally as an LC-resonant clock buffer. Case III and IV are degenerate cases when the input noise and the inherent noise are comparable. Since the spectral roll-off from the input signal is 20dB/dec, the two cases differ in the noise bandwidth (from a PLL) of the input signal. In case III where the bandwidth is low, the resulting jitter remains roughly constant for various current ratios because the two noise sources compensate. In case IV, if the input noise bandwidth is comparable or greater than the bandwidth of the LC tank, adapting the current ratio leads to an optimum jitter.

An automated tuning technique is proposed that adaptively maximizes the amplitude of the output clock. The signal amplitude is determined by an analog peak detector whose output feeds a current-controlled oscillator (CCO). The design shown in Fig. 9.6.2 digitizes the output swing by determining the frequency of the CCO.

The design is fabricated in 0.13µm CMOS. The dimensions of the main blocks are marked on the micrograph in Fig. 9.6.7. Fig. 9.6.4 shows the measurement setup. A pulse generator provdes the input clock and a noise generator adds white Gaussian noise at the input to verify the tradeoff. In this testchip, a digital oscilloscope is used as the jitter detector. Several techniques have been previously proposed to effectively measure jitter [6,7]. External software controls the feedback, maximizing the output swing.

The resonant frequency of the clock buffer has a range of 1.29 to 1.61GHz controlled by a 3-bit digitally adjustable capacitor. When the input frequency is 1.42GHz (close to the resonant frequency as the digital setting = 4), frequency control settings are swept while configuring the buffer as an injection-locked oscillator. The voltage amplitude of the output clock degrades as the LC resonant frequency is tuned away from the input frequency, as shown in Fig. 9.6.5. Because of the monotonicity of the result, a basic software algorithm allows us to digitally adapt the resonant frequency.

Figure 9.6.6(a) shows the jitter optimization results in measurement which match cases I, II, and IV of Fig. 9.6.3. A small (~1%) supply noise is induced by stimulating several inverters near the clock buffer. The current setting is swept and the output jitter is measured. With no added noise on the clean input clock from a reference generator, the optimal current setting favors that of a resonant buffer (cross-mark curve in Fig. 9.6.6(a)). The jitter is relatively insensitive to the setting because it is close to the measurement noise floor. As the buffer is configured to an injection-locked oscillator, the jitter increases because more buffer inherent noise is passed to output and slight injection pulling effect. A white Gaussian noise, whose bandwidth is greater than the on-chip LC tank, is added at the clock input. The noise magnitude is sufficient to increase the input clock jitter to σ_{jitter}=3.36ps. An optimum output jitter exists with the current ratio configured at ~80% (square-mark curve in Fig. 9.6.6(a)), which corresponds to case IV. If the noise is further increased on the input clock, the current configuration of the clock buffer eventually favors a fully injection-locked oscillator (circle-mark curve in Fig. 9.6.6(a)). Interestingly, due to the high-Q filtering of injection locked oscillator, the measured jitter of injection-locked oscillator does not vary substantially with different amounts of input clock jitter.

The jitter measurement is repeated with different total current for the clock buffer as shown in Fig. 9.6.6(b). For a fair jitter comparison, the output swing of the buffer is kept constant by increasing the swing of the input signal with larger tail current. Hence, the measured input rms jitter is 3.46ps, 3.19ps, and 2.92ps for cases of 1×, 1.15×, and 1.25× power, respectively. As expected, the increasing current improves the jitter performance. By operating the buffer at the optimum, the jitter is better than operating the clock buffer with 25% greater power when it is configured as purely an injection-locked oscillator or LC-resonant clock buffer. This paper shows that adaptability is an important part of LC-based buffer design. Otherwise, substantial power penalty results if the buffer configuration is improperly chosen.

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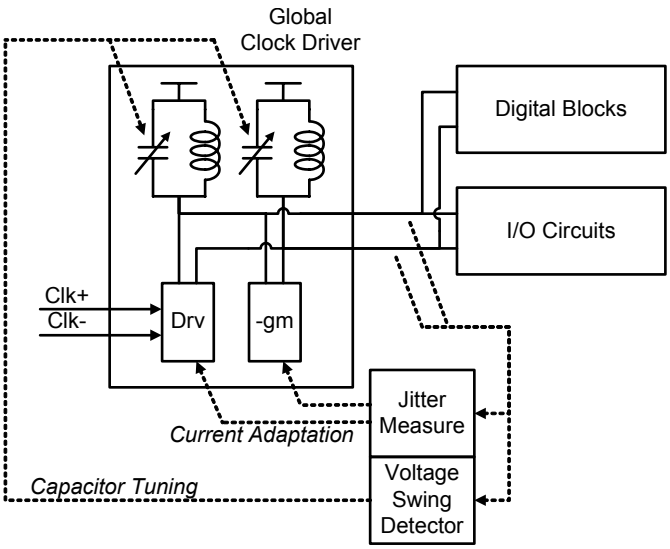

Figure 9.6.1: System diagram.

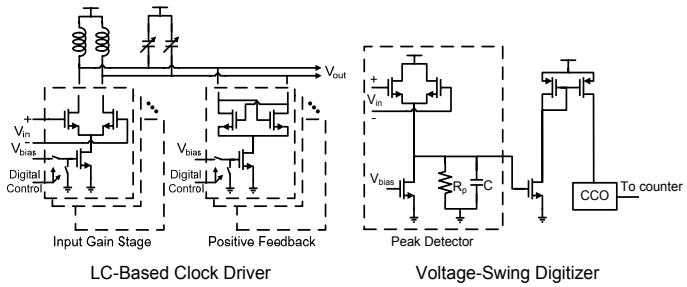

Figure 9.6.2: Schematic of LC-based clock driver and voltage-swing digitizer.

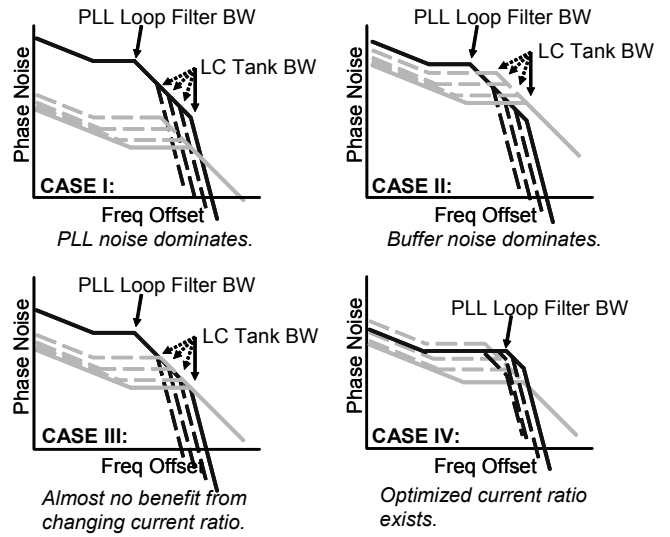

Figure 9.6.3: Jitter-optimized current ratio for 4 different cases.

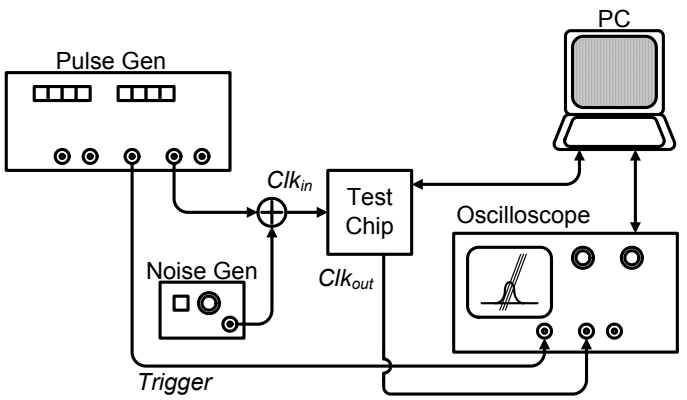

Figure 9.6.4: Measurement setup.

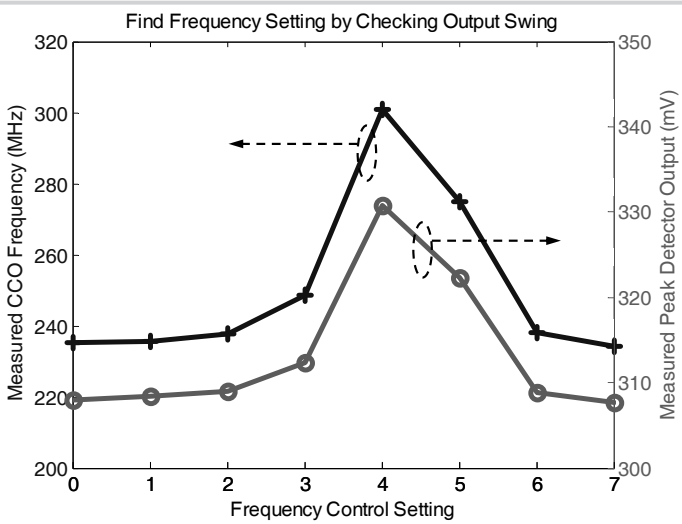

Figure 9.6.5: Measurement results of voltage-swing digitizer when input frequency is 1.42GHz.

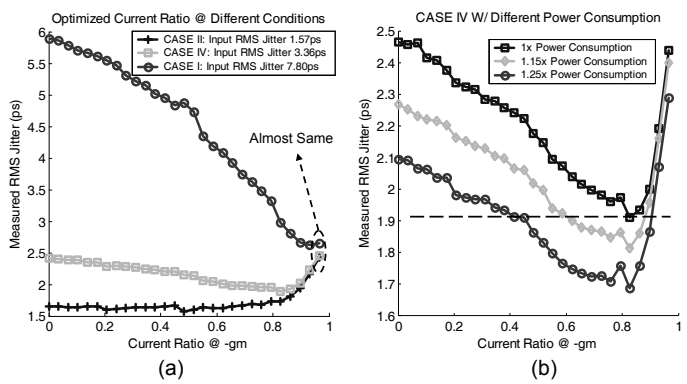

Figure 9.6.6: Optimized current-ratio measurement (a) different amounts of input noise and (b) different power consumption.

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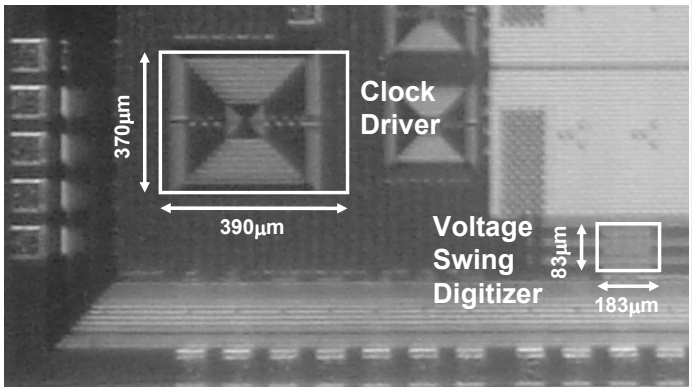

Figure 9.6.7: Die micrograph.

